LISTING OF CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

1. (currently amended) A semiconductor device, comprising:

a substrate including a dopant of a first polarity;

a first semiconducting structure including a dopant of a second polarity and disposed over said substrate, said first semiconducting structure having substantially planar top and side surfaces;

a first junction formed between said first semiconducting structure and said substrate, said first junction having an area [having]with at least one lateral dimension less than about 75 nanometers.

2. (currently amended) The semiconductor device in accordance with claim 1, further comprising:

a second semiconducting structure including a dopant of said first polarity formed on said first semiconducting structure said second semiconducting structure having substantially planar top and side surfaces; and

a second junction formed between said first semiconducting structure and said second semiconducting structure, said second junction having a length and a width, and said second junction having an area [having]with at least one lateral dimension less than about 75 nanometers.

3. (currently amended) The semiconductor device in accordance with claim [1]2, wherein said first semiconducting structure further comprises a plurality of epitaxial semiconducting base lines substantially parallel to each other, and said [first]second semiconducting structure further comprises a plurality of [first] second semiconducting lines substantially parallel to each other and at a predetermined angle to said plurality of epitaxial semiconducting base lines.

4. (currently amended) The semiconductor device in accordance with claim 3, wherein said plurality of epitaxial semiconducting lines and said [first] plurality of second semiconducting lines form an array of bipolar junction transistors having at least one junction having a junction area [having]with at least one lateral dimension less than about 75 nanometers.

5. (currently amended) A semiconductor device, comprising:

a substrate;

a base epitaxial semiconducting layer including a dopant of a first polarity disposed over said substrate;

a first semiconducting layer including a dopant of a second polarity disposed over said substrate; and

a first junction formed between said base epitaxial semiconducting layer and said first semiconducting layer, said first junction having an area [having]with at least one lateral dimension less than about 75 nanometers.

6. (currently amended) The semiconductor device in accordance with claim 5, further comprising:

a second semiconducting layer including a dopant of said second polarity formed over said base epitaxial semiconducting layer; and

a second junction formed between said epitaxial semiconducting base layer and said second semiconducting layer having a length and a width, and said second junction having an area [having]with at least one lateral dimension less than about 75 nanometers.

7. (original) The semiconductor device in accordance with claim 6, wherein said first semiconducting layer further comprises a first epitaxial semiconducting layer, wherein said base epitaxial semiconducting layer, said first epitaxial semiconducting layer, and said second semiconducting layer form a vertical bipolar transistor.

8. (original) The semiconductor device in accordance with claim 6, further comprising an electrically conductive layer forming an ohmic contact to a portion of said base epitaxial semiconducting layer, and said electrically conductive layer forming a Schottky barrier to a portion of either said first or said second semiconducting layers, whereby a Schottky diode clamped bipolar junction transistor is formed.

9. (original) An integrated circuit comprising:

at least one semiconductor device of claim 6; and

a transistor control circuit coupled to said at least one semiconductor device.

10. (original) The semiconductor device in accordance with claim 5, wherein said substrate further comprises a semiconductor substrate having a dopant of said second polarity, wherein said semiconductor substrate forms said first semiconductor layer.

11. (original) The semiconductor device in accordance with claim 5, wherein said base epitaxial semiconducting layer further comprises a plurality of epitaxial semiconducting base lines substantially parallel to each other, and said first semiconducting layer further comprises a plurality of first semiconducting lines substantially parallel to each other and at a predetermined angle to said plurality of epitaxial semiconducting base lines.

12. (original) The semiconducting device in accordance with claim 11, further comprising a plurality of second semiconducting lines substantially parallel to each other and at a predetermined angle to said plurality of epitaxial semiconducting base lines.

13. (currently amended) The semiconducting device in accordance with claim 11, wherein said substrate further comprises a dielectric layer disposed between said substrate and said plurality of epitaxial semiconducting base lines.

14. (original) The semiconducting device in accordance with claim 11, wherein said epitaxial semiconducting base lines and said first and second semiconducting lines form a hexagonal array.

15. (original) The semiconductor device in accordance with claim 11, wherein said plurality of first semiconducting lines are substantially mutually orthogonal to said plurality of epitaxial semiconducting base lines.

16. (original) The semiconductor device in accordance with claim 11, wherein said predetermined angle is between about 20 degrees and about 90 degrees.

17. (original) The semiconductor device in accordance with claim 11, wherein said plurality of first semiconducting lines and said plurality of epitaxial semiconducting base lines form a diode array having an areal density in the range from about 0.2 Tera diodes/cm^2 to about 10.0 Tera diodes/cm^2.

18. (original) The semiconductor device in accordance with claim 11, wherein said plurality of first semiconducting lines and said plurality of epitaxial semiconducting base lines form a bipolar junction transistor array having an areal density in the range from about 0.2 Tera transistors/cm^2 to about 10.0 Tera transistors/cm^2.

19. (original) The semiconductor device in accordance with claim 5, wherein said first junction further comprises an area of less than about 15,000 square nanometers.

20. (original) The semiconductor device in accordance with claim 5, wherein said substrate further comprises a dielectric layer disposed between said substrate and said base epitaxial semiconducting layer.

21. (original) The semiconductor device in accordance with claim 5, wherein said base epitaxial semiconducting layer further comprises a thickness in the range from about 1.0 nanometer to about 1,000 nanometers.

22. (original) An electronic device, comprising:

an integrated circuit including at least one semiconductor device of claim 5.

23. (original) A computer system, comprising:

a microprocessor;

an electronic device including at least one semiconductor device of claim 5 coupled to said microprocessor; and

memory coupled to said microprocessor, said microprocessor operable of executing instructions from said memory to transfer data between said memory and the electronic device

24. (original) The computer system in accordance with claim 23, wherein said electronic device is a storage device.

25. (original) The computer system in accordance with claim 23, wherein said electronic device is a display device.

26. (currently amended) The computer system in accordance with claim 23, wherein said memory further comprises an integrated circuit including at least one semiconductor device having:

a substrate;

[an] a base epitaxial semiconducting layer including a dopant of a first polarity disposed over said substrate;

a first semiconducting layer including a dopant of a second polarity disposed over said substrate; and

a first junction formed between said base epitaxial semiconducting layer and said first semiconducting layer, said first junction having an area [having]with at least one lateral dimension less than about 75 nanometers.

27. (original) The computer system in accordance with claim 26, wherein said base epitaxial semiconducting layer further comprises a plurality of epitaxial semiconducting base lines substantially parallel to each other, and said first semiconducting layer further comprises a plurality of first semiconducting lines substantially parallel to each other and at a predetermined angle to said plurality of epitaxial semiconducting base lines.

28. (currently amended) The computer system in accordance with claim 23, wherein said microprocessor further comprises an integrated circuit including at least one semiconductor device having:

a substrate;

[an] a base epitaxial semiconducting layer including a dopant of a first polarity disposed over said substrate;

a first semiconducting layer including a dopant of a second polarity disposed over said substrate; and

a first junction formed between said base epitaxial semiconducting layer and said first semiconducting layer, said first junction having an area [having] with at least one lateral dimension less than about 75 nanometers.

29. (original) The computer system in accordance with claim 28, wherein said base epitaxial semiconducting layer further comprises a plurality of epitaxial semiconducting base lines substantially parallel to each other, and said first semiconducting layer further comprises a plurality of first semiconducting lines substantially parallel to each other and at a predetermined angle to said plurality of epitaxial semiconducting base lines.

30. (currently amended) A bipolar junction transistor, comprising:

a semiconductor substrate having a substantially planar surface including a dielectric layer formed on or within said substrate;

a first epitaxial semiconducting structure including a dopant of a first polarity disposed on said dielectric layer, said first epitaxial semiconducting structure having an area formed in a plane parallel to said substrate of less than about 15,000 square nanometers;

a second epitaxial semiconducting structure including a dopant of a second polarity formed on said first epitaxial semiconductor structure, said second epitaxial semiconducting structure having an area formed in a plane parallel to said substrate of less than about 15,000 square nanometers;

a third epitaxial semiconducting structure including a dopant of said first polarity formed on said second epitaxial semiconductor sturcture, said third epitaxial structure having an area formed in a plane parallel to said substrate of less than about 15,000 square nanometers; and

an electrically conductive layer forming an ohmic contact to a portion of said second epitaxial semiconducting structure, and said electrically conductive layer forming a Schottky barrier to a portion of either said first or said third epitaxial semiconducting structures, whereby a Schottky diode clamped bipolar junction transistor is formed.

31. (currently amended) A bipolar junction transistor, comprising:

a semiconductor substrate having a substantially planar surface including a dielectric layer formed on said substrate

an epitaxial semiconducting structure formed on said dielectric layer, said epitaxial structure having an area [having] with at least one lateral dimension less than about 75 nanometers, and forming a base region of the bipolar junction transistor;

a first polycrystalline semiconducting structure, formed on at least a portion of said epitaxial structure, said first polycrystalline structure having an area [having] with at least one lateral dimension less than about 75 nanometers, and forming an emitter region of the bipolar junction transistor; and

a second polycrystalline semiconducting structure formed on at least a portion of said epitaxial structure, said second polycrystalline structure having an area [having] with at least one lateral dimension less than about 75 nanometers, and forming a collector region of the bipolar junction transistor.

32. (currently amended) A diode array, comprising:

a silicon semiconductor wafer;

an insulating layer disposed over said silicon wafer;

a plurality of epitaxial semiconducting structures having an area [having] with at least one lateral dimension less than about 75 nanometers, said plurality of epitaxial structures disposed over said insulating layer; and

a plurality of polycrystalline semiconducting structures having an area [having] with at least one lateral dimension less than about 75 nanometers, said plurality of polycrystalline structures in contact with said plurality of epitaxial structures, forming an array of semiconducting junctions.

33. (currently amended) A semiconductor device, comprising:

a substrate;

an epitaxial semiconducting structure formed on said substrate;

a polycrystalline semiconducting structure; and

means for forming a first semiconducting junction between said epitaxial semiconductor structure and said polycrystalline semiconducting structure, said semiconducting junction having an area [having]with at least one lateral dimension less than about 75 nanometers.

34. (currently amended) The semiconductor device in accordance with claim 33, further comprising: means for forming a second semiconducting junction between said epitaxial semiconductor layer and said substrate, said second semiconducting junction having an area [having] with at least one lateral dimension less than about 75 nanometers.

35. - 56. (canceled)

57. (new) The semiconductor device in accordance with claim 5, wherein said substrate further comprises a dielectric layer disposed between said substrate and said first semiconducting layer.

58. (new) The semiconducting device in accordance with claim 11, wherein said substrate further comprises a dielectric layer disposed between said substrate and said plurality of first semiconducting lines.